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EXAMINER	
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ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/680,105	ABE ET AL.	
	Examiner	Art Unit	
	STEVEN D. RADOSEVICH	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13* is/are allowed.

6)☒ Claim(s) *1-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/2/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-14 are present within this instant examination, which is in response to applicant's correspondence on 1/2/2008.

Priority

Priority is claimed for this application to 10/09/2002 as noted within prior examinations and will be used for this examination.

Drawings

Acknowledgment is made that the newly corrected drawings are accepted since at this time no issues appear to be present that would require and objection or further correction.

Information Disclosure Statement

Acknowledgment is made that a further (new) IDS has been submitted by the applicant and has been considered at this time. Examiner notes that a single foreign patent document is disclosed within the new IDS; Document num 2001-142918 from Japan with only an English abstract.

Response to Arguments

Applicant's arguments filed 1/2/08 have been fully considered but they are not persuasive. Applicant respectfully argues the following:

i. With respect to claims 5 and 6 and the 35 U.S.C. 112, second paragraph issues that a person of ordinary skill in the art would find claims 5 and 6 clear, that the claims clearly describe the priority order to the validation items to be extracted by the extracting unit.

ii. A person of ordinary skill in the art would not have recognized expressing Boolean functions within a binary decision diagram at the time Buckley Jr was invented.

With respect to argument i, the examiner would like to first direct applicant to the M.P.E.P. section 2111 which requires that the examiner give "the broadest reasonable interpretation" the claims "consistent with the specification" it also warns that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The claims must stand on their own. Furthermore the extraction of the validation items and/or the priority order in which the validation items are extracted was and is not the bases of the 35 U.S.C. 112, second paragraph rejection of the claims. The rejection(s) are and were bases on it being unclear as to which of the plurality of extracted validation items is used in the generation of the input/output sequence. Examiner notes that after the extraction of a plurality of validation items (claim 6) based on a priority (claim 5), the input/output sequence is still claimed to be based on the validation item (claim 1), indicating a single or one validation item of the plurality extracted without identification as to how or which validation item is selected for use in the generating of the input/output sequence. Therefore the **35 U.S.C. 112 second paragraph rejections of claims 5 and 6 is not withdrawn**, are still rejected under 35 U.S.C. second paragraph, since the arguments were not persuasive.

With respect the argument ii, examiner directs applicant to the June 1978 paper by Sheldon B Akers titled "Binary Decision Diagrams" predating Buckley Jr and used bellow within the 103 rejection(s).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "the functional configuration information" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes there is no prior introduction of "a functional configuration information" from which "the functional configuration information" can be dependent upon or referencing.

Double Patenting

Claim 14 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 13. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4, 9, 11, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ruiz et al (U.S. Patent 6195776 B1).

1. As per claims 1, 11, and 12 Ruiz teaches comprising:

A first input for inputting functional configuration information on the functional devices and connections among the functional devices (hardware description language (HDL), register transfer level (RTL), Verilog, and VHDL in column 1 lines 45-56, HDL in column 3 lines 1-2, receiving an HDL in the abstract, and 201 in figure 1A);

A second input unit for inputting a condition for the input/output sequence (performance constraints in column 3 lines 3-10); and

A first generating unit that generates a validation item function based on the functional configuration information and the condition ("generic" netlist in column 3 lines 10-15);

An extracting unit that extracts a combination of functional devices as a validation item, from the validation item function (cell library 204 in column 3 lines 17-25 and figure 1A); and

A second generating unit that generates the input/output sequence based on the validation item (automatic test pattern generation (ATPG) in column 3 lines 35-40).

2. As per claim 3, Ruiz teaches wherein the condition includes a resource constraint condition for the functional devices (performance constraints in column 3 lines 3-10).

3. As per claim 4, wherein the condition includes a condition that limits the functional devices to be included in the validation item (performance constraints in column 3 lines 3-10).

4. As per claim 9, Ruiz teaches wherein the apparatus is connected, via a network, to an information terminal from which the functional configuration information and the condition are input and to which the validation item and the input/output sequence are output (see figures 1 and 2, computer system in the abstract).

Claim Rejections - 35 USC § 103

Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Ruiz et al (U.S. Patent 6195776 B1) as applied to claim 1 above, and further in view of Sheldon B. Akers (Binary Decision Diagram, IEEE, June 1978).

5. As per claim 2, Ruiz teaches as described above in detail: a first input, a second input, a fist generating, an extracting, and a second generating. Ruiz further teaches wherein the descriptions of the circuit are expressed with Boolean equations.

Ruiz does not specifically teach wherein the validation item function is expressed by a binary decision diagram.

However Sheldon teaches wherein the Boolean equations or functions can be expressed as binary decision diagram within an analogous art (see all figures, the Introduction, and the fist paragraph on page 510).

Therefore one or ordinary skill within the art at the time the invention was made would have been motivated to modify Ruiz so as to express the Boolean equations or functions as binary decision diagrams as taught by Sheldon since one need only simply proceed downward thought the diagram as taught within Sheldon (page 509 within the Binary Decision Diagrams section describing figure 1) allowing for greater easy to propagate through a Boolean expression, allow for visual construction of the expression or equation to ensure proper expression or equation, or allow easy backtracking within the equation if an error is made while propagating thought the equation rather than starting over.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ruiz et al (U.S. Patent 6195776 B1) as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art (AAPA) as disclosed (20040073859 A1).

6. As per claim 7, Ruiz teaches as described above a first input, a second input, a fist generating, an extracting, and a second generating.

Ruiz does not specifically teach:

> A converting unit that converts a functional block diagram of the target apparatus into a graph including a plurality of nodes and a plurality of edges, wherein the graph is input to the apparatus as the functional configuration information.

However AAPA teaches that conventionally prior to the invention a method existed of extracting an input/output sequence from a functional block diagram created by using a predetermined description language. According to this method, the functional block diagram expresses the apparatus to be validated (tested) as a functional device and a data flow between the functional devices. A graph is created by replacing the functional devices and the data flow with nodes edges, respectfully (paragraph 7).

Therefore it would have been obvious to one of ordinary skill within the art at the time the invention was made to have been motivated to have a converting unit convert a functional block diagram of the target apparatus into a graph including a plurality of nodes and a plurality of edges, wherein the graph is input to the apparatus as the functional configuration information within Ruiz since doing so at the time of the invention was the conventional known to work method of preparing the functional configuration information for generating an input/output sequence (AAPA paragraphs 6-7).

Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruiz et al (U.S. Patent 6195776 B1) as applied to claim 1 above.

7. As per claim 8, Ruiz teaches as described above a first input, a second input, a fist generating, an extracting, and a second generating.

Ruiz does not specifically teach:

> A third input unit for inputting a validation environment that defines a flow of data that is input to and output from the target apparatus, wherein the second

generating unit that generates the input/output sequence, based on the validation environment and the validation item.

However those of ordinary skill within the art at the time the invention was made would recognize that an input unit for inputting a validation environment that defines a flow of data that is input to and output from the target apparatus, wherein the generating unit that generates the input/output sequence, based on the validation environment and the validation item is well know.

Ruiz teaches the claimed invention except for a third input for inputting an environment since this third input of the environment is already included within the performance constraints taught within Ruiz. It would have been obvious to one having ordinary skill in the art at the time the invention was made to independently input the environment separate from performance constraints, since it has been held that constructing a formally integral structure in various elements involves only routine skill in the art. *Nerwin* v. *Erlichman,* 168 USPQ 177, 179.

8. As per claim 10, Ruiz teaches wherein the apparatus is connected, via a network, to an information terminal from which the functional configuration information, the condition, and the validation environment are input and to which the validation item and the input/output sequence are output (see figures 1 and 2, computer system in the abstract).

Claim Rejections - 35 USC § 103

Claims 1, 9, 10, 11, and 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Angilivelil (U.S. Publication 20040025123 A1), Crouch et al (U.S. Patent 5592493), and further in view of Kapur et al (U.S. Patent 6385750 B1).

9. As per claims 1, 11, and 12, Angilivelil teaches comprising:

A first input for inputting functional configuration information on the functional devices and connections among the functional devices (design in "design associated with the IC chip" within the abstract; netlist or design netlist in paragraph 0021; design description in paragraph 0025);

A second input unit for inputting a condition for the input/output sequence (performance criteria in the abstract; target performance data and input/output requirements in paragraph 0025); and

A first generating unit that generates a validation item function based on the functional configuration information and the condition (critical paths in abstract and paragraphs 0008; critical path data in paragraph 0025).

Angilivelil does not specifically teach:

An extracting unit that extracts a combination of functional devices as a validation item, from the validation item function; and

A second generating unit that generates the input/output sequence based on the validation item.

However Crouch teaches tracing back through a logic to determine all devices, paths, and cells required for testing the validation item (critical path), since they effect

the path (see figure 14, column 12 lines 55-60, and column 13 lines 1-8) in an analogous art. The tracing back within Crouch reads on the extracting and validation item since within tracing back requires all the logic, devices, and connections required for testing the validation item (critical path).

Therefore one of ordinary skill within the art at the time the invention was made would have been motivated to modify Angilivelil to include the tracing back of Crouch so as to have control while testing since other circuitry, logic, devices, and connections having an influence upon that which is being tested must also be controlled and/or established as indicated within Crouch (column 13 lines 5-12 and 24-34) so as to conduct useful testing.

Angilivelil as modified however does not specifically teach:

A second generating unit that generates the input/output sequence based on the validation item.

However Kapur teaches systems including automatic test pattern generation (ATPG) for analyzing various representations of netlist designs and generating test patterns therefrom (column 1 lines 41-50) within an analogous art.

Therefore one of ordinary skill within the art at the time the invention was made would have been motivated to further modify Angilivelil as modified to include the ATPG as taught within Kapur to generate an input/output sequence based on the validation item so as to be fully functional and facilitate testing as indicated by Kapur (column 1 lines 42-50) for that which is to be tested.

10. As per claim 5, Angilivelil teaches wherein the extracting unit extracts a plurality of validation items based on a priority of each of the validation items, the priority being calculated based on a priority assigned to each of the functional devices (critical paths in abstract and paragraphs 0008).

11. As per claim 6, Angilivelil teaches wherein the extracting unit extracts n or less validation items, where n or less validation items extracted is a positive integer larger than one (critical paths in abstract and paragraphs 0008).

12. As per claim 9, Angilivelil teaches wherein the apparatus is connected, via a network, to an information terminal from which the functional configuration information and the condition are input and to which the validation item and the input/output sequence are output (see figure 1).

13. As per claim 10, Angilivelil teaches wherein the apparatus is connected, via a network, to an information terminal from which the functional configuration information, the condition, and the validation environment are input and to which the validation item and the input/output sequence are output (see figure 1).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Angilivelil (U.S. Publication 20040025123 A1), Crouch et al (U.S. Patent 5592493), and further in view of Kapur et al (U.S. Patent 6385750 B1) as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art (AAPA) as disclosed (20040073859 A1).

14. As per claim 7, Angilivelil as modified teaches as described above a first input, a second input, a fist generating, an extracting, and a second generating.

Angilivelil does not specifically teach:

A converting unit that converts a functional block diagram of the target apparatus into a graph including a plurality of nodes and a plurality of edges, wherein the graph is input to the apparatus as the functional configuration information.

However AAPA teaches that conventionally prior to the invention a method existed of extracting an input/output sequence from a functional block diagram created by using a predetermined description language. According to this method, the functional block diagram expresses the apparatus to be validated (tested) as a functional device and a data flow between the functional devices. A graph is created by replacing the functional devices and the data flow with nodes edges, respectfully (paragraph 7).

Therefore it would have been obvious to one of ordinary skill within the art at the time the invention was made to have been motivated to have a converting unit convert a functional block diagram of the target apparatus into a graph including a plurality of nodes and a plurality of edges, wherein the graph is input to the apparatus as the functional configuration information within Angilivelil since doing so at the time of the invention was the conventional known to work method of preparing the functional configuration information for generating an input/output sequence (AAPA paragraphs 6-7).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i. Funkui (U.S. Patent 6470468 B1) discloses netlist information and condition of constraints being input into a test pattern generator.

ii. Fujitsu (2001-142918 JP) as provided within the IDS discloses generating priority to be verified about a hardware description language (netlist, HDL, VHDL, or Verilog), along with graphs for simplification by optimizing processing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN D. RADOSEVICH whose telephone number is (571)272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACQUES H LOUIS-JACQUES/ Steven D. Radosevich

Supervisory Patent Examiner, Art Unit 2117

Examiner
Art Unit 2117